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DESCRIPTION

Method for storing video signals

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Technical field

The invention relates to a method for storing
10 video signals with the aid of a random access
memory (SDRAM) that is operated synchronously
during writing and reading, there being connected
downstream of the random access memory a further
memory (FIFO) with different frequencies for
15 writing and reading.

Background of the invention

20 Television equipment and systems often require
storage of video signals, and reading and writing
are to be performed with different clocks. This is
the case for example in film scanners and in
synchronising devices. Memory modules in which
25 reading can be effected with a different clock
from writing are so-called FIFOs (First-In First-
Out) for example. The latter have the disadvantage
however, that they are available for the large
capacity required for the abovementioned purposes
30 only with a considerable outlay. Moreover, the
maintenance of the temporal sequence of the
signal, that is to say of the pixels, which is
provided in the case of FIFOs considerably
restricts their use. Although random access
35 memories (RAMs) are more advantageous in this
respect, the addressing and changeover between
writing and reading operation reduces the speed.

Summary of the invention

The method according to the invention consists in
5 the fact that the video signals to be stored are
divided into a plurality of parallel data streams,
that the data streams are time-compressed in such
a way that the compressed data streams take up
10 only a part of a predetermined write-read cycle
for the random access memory, that data streams
read from the random access memory are conducted
via the further memory and combined to form video
signals.

15 The method according to the invention enables
rapid reading and writing, so that even video
signals with very high bit rates can be stored.
Moreover, SDRAMs with large capacities can be
obtained at low cost. In the case of the method
20 according to the invention, the rapid writing and
reading is made possible in particular by virtue
of the fact that not every memory location need be
addressed individually, rather only one bank
address is used for a data block comprising 512
25 pixels, for example, which are read again in the
same sequence. Nevertheless, the method according
to the invention is extremely flexible and enables
the video signals to be read in a manner largely
independent of the clock and the structure (number
30 of pixels, number of lines, interline or
progressive) of the video signals supplied.

In order to enable reading of the video signals
faster than writing, the method according to the
35 invention may provide for the write-read cycle to
comprise a write period and at least one read
period. In this case, it has proved to be

advantageous if the write-read cycle comprises a write period and three read periods.

An advantageous refinement of the method according to the invention consists in the fact that the write or read periods in each case contain, prior to the writing or reading, respectively, control time segments for setting the random access memory for writing or reading, respectively, and, after the write or read periods, respectively, control time segments for terminating the writing or reading, respectively. In said time segments, all the commands required for the subsequent writing or reading are fed to the random access memories.

In this case, it may furthermore be provided that the random access memory is furthermore refreshed in the time segments. This refinement can be developed such that in the control time segments preceding the writing or reading, the following code sequence is fed to the random access memory: NOPS, PALL, NOPS, REF, ACTV, ACTV, NOPS.

By virtue of the fact that the control time segments contain defined signals - in contrast to the continuously changing video data - the signals in the control time segments can readily be utilised for the synchronisation of digital measurement and test devices.

In a method embodied in practice, it was furthermore provided that in the control time segments after writing or reading, the following code sequence is fed to the random access memory: BST, PALL, REF, NOPS.

Details of these code sequences depend on the respective embodiments of the SDRAMs.

The division of the video signals (demultiplex) may be chosen differently depending on requirements made of speed, made of quantity of video data to be stored, and depending on the SDRAM used. In a method carried out in practice, it has proved expedient for the video signals to be divided pixel by pixel.

Brief description of the drawing

An exemplary embodiment of the invention is illustrated in the drawing using a plurality of figures and is explained in more detail in the description below. In the figures:

Figure 1 shows an arrangement for carrying out the method according to the invention,

Figure 2 diagrammatically shows the illustration of the division of the video signals into a plurality of data streams, and

Figure 3 diagrammatically shows write and read operations and also the intervening control of the SDRAM.

Description of the exemplary embodiments

Digital video signals are fed to the arrangement according to Figure 1 via an input 2, which signals are divided into four parallel data streams a, b, c, d in a circuit 3, which data streams are delayed relative to one another in each case by the duration of a pixel. In a buffer memory 3' - designated as PREFIFO in Figure 1 -

every fourth pixel is taken from the data streams a, b, c, d, thereby producing compressed data streams A, B, C, D. To that end, the circuit 3 and the buffer memory 3' are clocked with a clock CKA (also called Masterclock). The buffer memory 3' receives suitable control signals WR_EN and RD_EN, which bring about the writing of every fourth pixel and the reading of each stored pixel.

10 This operation is illustrated diagrammatically in Figure 2, the duration of a television line being indicated in line H using blanking pulses. Owing to the large ratio of the line period to the duration of a pixel, all of the signals and data
15 streams are shown interrupted in Figure 2.

The lines a to d show the data streams which are in each case delayed by the duration of a pixel and are designated identically in Figure 1. In this case, the pixels are numbered consecutively starting from 0. In this form, the data streams a to d are fed to the buffer memory 3' (Figure 1). Every fourth pixel respectively contained in the data stream a to d is written and read with the
20 clock CKA - that is to say, in Figure 2, pixels 3 and 7 from data stream a, pixels 2 and 6 from data stream b, etc. As a result, the data streams A, B, C and D are produced with the same "pixel clock" CKA. Since they each contain only every fourth
25 pixel, they are correspondingly time-compressed with respect to the data streams a to d.

A respective colour component of a pixel is reproduced by means of a data word having a width
35 of ten bits. However, other bit widths are also possible. For greater clarity in the illustration, the processing of a plurality of colour components is not discussed in detail in the exemplary

embodiment. It is to be assumed that a plurality of data streams, for example for R, G and B or Y, CR and CB, are correspondingly processed in parallel. Equally, in the case of supplied video
5 signals which form the basis for a progressive scanning and are later used as video signals with interline, it is possible to provide separate memories or memory areas for the even-numbered and odd-numbered lines.

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The data streams indicated in lines A to D in Figure 2 are then written to the random access memory 1 and are buffer-stored there according to the invention. The SDRAM 1 receives addresses ADDR
15 and control data CONTR from an SDRAM controller 8. Moreover, the SDRAM 1 and the SDRAM controller 8 receive the clock CKA. This clock serves for writing and reading in the SDRAM 1.

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Connected to the SDRAM 1 is a FIFO memory 4, to which the data streams read from the SDRAM are written with the clock CKA. A clock CKB serves for reading from the FIFO memory 4. The said clock is part of the studio standard and is not synchronous
25 with the clock CKA. The clocks CKA and CKB and also reset signals WRES and PRES are fed to a further control device 7. The occupancy of the FIFO memory 4 is determined from the two clocks CKA and CKB. If the FIFO memory 4 threatens to
30 overflow or become empty, corresponding items of information are passed to the SDRAM controller 8 which fills the FIFO memory 4 by reading further data or initially prevents the reading of further data.

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An entire write-read cycle illustrated in Figure 3 contains a write period WR and read periods READ1 to READ3. Each of these write and read periods is

assigned a time segment WP and RP, respectively,
for preparing for the writing and reading,
respectively, and a time segment WF and RF,
respectively, for terminating the writing and
5 reading, respectively. The memory content of the
SDRAM is also refreshed during these time
segments.

In the SDRAM controller 8, command sequences are
10 programmed for the write and read preparation WP
and RP, respectively, and also for the termination
WF and RF of the respective operation, which
command sequences are adapted to the use of the
respective SDRAM module. In a practical embodiment
15 of the invention using an SDRAM of the
MB81F64842C-102 type from Toshiba, the following
commands were chosen:

WP: NOPs, PALL, NOPs, REF, ACTV, ACTV, NOPs,
WR: WRIT, (NOPs),
20 WF: BST, PALL, REF, NOPs,
RP: NOPs, PALL, NOPs, REF, ACTV, ACTV, NOPs,
RD: READ, (NOPs),
RF: BST, PALL, REF, NOPs.